CLAIMS

What is claimed is:

~~1. A cell structure comprising:~~

~~a first junction and a second junction separated by a channel region, the first and second junctions being in a body region;~~

~~a first and a second floating gates over the channel region, and~~

~~a select-gate having a portion between the first and second floating gates, the select-gate also extending over at least a portion of each of the two floating gates.~~

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2. The cell structure of Claim 1 wherein the first floating gate extends over a first portion of the channel region and over a portion of the first junction, and the second floating gate extends over a second portion of the channel region and over a portion of the second junction.

3. The cell structure of Claim 2 wherein the portion of select-gate between the two floating gates extends over a third portion of the channel region between the first and second channel portions.

4. The cell structure of Claim 3 wherein the first, second, and third portions of the channel region do not overlap with one another, and the first, second, and third channel portions together form the entire channel region between the first and second junctions.

6 5. The cell structure of Claim 2 wherein each of the first and second floating gates has at least one slanted surface forming a sharp edge.

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6. The cell structure of Claim 5 further comprising an inter-polysilicon dielectric layer for insulating the first and second floating gates from the select-gate, the inter-polysilicon dielectric layer being thinnest between the sharp edge of each of the two floating gates and the select-gate.

7. The cell structure of Claim 1 wherein the select-gate extends over and beyond the first and second floating gates.

8. The cell structure of Claim 1 further comprising:

an insulating layer for insulating the first and second floating gates from their underlying channel regions; and

an insulating layer for insulating the select-gate from the select-gate's underlying channel region;

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9. The cell structure of Claim 1 wherein each of the ~~first~~ first and second floating gates is capable of storing one bit of information.

10. The cell structure of Claim 1 wherein by applying a first positive voltage to the first junction and a second positive voltage to the select-gate and grounding the second junction and the body region a potential on the first floating gate is decreased.

11. The cell structure of Claim 10 wherein the potential on the first floating gate is decreased through hot-carrier injection mechanism.

12. The cell structure of Claim 1 wherein by applying a first positive voltage to the second junction and a second positive voltage to the select-gate and grounding the first junction and the body region a potential on the second floating gate is decreased.

13. The cell structure of Claim 12 wherein the potential on the second floating gate is decreased through hot-carrier injection mechanism.

14. The cell structure of Claim 1 wherein by applying a positive voltage to the select-gate and grounding the first junction, the second junction, and the body region a potential of the first floating gate and a potential of the second floating gate are simultaneously increased.

15. The cell structure of Claim 14 wherein the potential of the first floating and the potential of the second floating gate are increased through tunneling mechanism.

16. The cell structure of Claim 1 wherein the amount of charge on the first floating gate is detected by applying a first positive voltage to the select-gate, a second positive voltage to the second junction and grounding the first junction and the body region.

17. The cell structure of Claim 1 wherein the amount of charge on the first floating gate is detected by applying a first positive voltage to the select-gate, a second positive voltage to the second junction, a third positive voltage to the first junction, and grounding the body region, wherein the second positive voltage is greater than the third positive voltage.

18. The cell structure of Claim 1 wherein the amount of charge on the first floating gate is detected by applying a first positive voltage to the select-gate, a second positive voltage to the second junction, grounding the body region, and measuring the voltage at the first junction while forcing a predetermined amount of current through the channel region.

~~19. The cell structure of Claim 1 wherein the body region is a first well of a first conductivity type, the first well being formed in a second well of a second conductivity type opposite the first conductivity type, the second well being formed in a substrate region of the first conductivity type, wherein the first and second junctions are of the second conductivity type.~~

~~20. The cell structure of Claim 19 wherein the first well is capable of being independently biased to a predetermined positive or negative or zero voltage.~~

21. The cell structure of Claim 1 wherein each of the first and second floating gates has at least one slanted surface forming a sharp edge, the at least one slanted surface of each of the first and second floating gates being either a side surface or a top surface of each of the first and second floating gates.

22. The cell structure of Claim 1 wherein two opposing side surfaces of each of the two floating gates are slanted forming two sharp edges.

23. The cell structure of Claim 1 wherein a top surface of each of the first and second floating gates is bowl-shaped forming two sharp edges.

24. The cell structure of Claim 1 wherein two opposing side surfaces of each of the two floating gates are slanted and a top surface of each of the two floating gates is bowl-shaped, the combination of the two slanted side surfaces and the bowl-shaped top surface forming two sharp edges.

25. The cell structure of Claim 1 wherein the cell is a source-side injection flash EEPROM cell having four operating terminals, the flash EEPROM cell being capable of storing two bits of information.

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~~26. The cell structure of Claim 7 in combination with other similar cell structures forming a virtual ground array, wherein the cells are serially connected along a plurality of rows and columns, the select-gates of the cells along each row being connected together forming a wordline, the first junction of cells along each column being connected together forming a continuous bitline, and the second junction of the cells along each column being connected together forming another continuous bitline.~~

~~27. The cell structure of claim 1 further comprising an inter-polysilicon dielectric layer for insulating the first and second floating gates from the select-gate, the inter-polysilicon dielectric having a weak region so that electrons can tunnel from the first and second floating gates to the select-gate.~~

~~28. A memory array comprising:~~

~~a plurality of cells arranged to form rows and columns of cells, each cell comprising:~~

~~a first junction and a second junction separated by a channel region, the first and second junctions being in a body region;~~

a first floating gate and second floating gate each having at least one slanted surface forming a sharp edge, the first floating gate extending over a first portion of the channel region and over a portion of the first junction, and the second floating gate extending over a second portion of the channel region and over a portion of the second junction;

a select-gate extending over and beyond the two floating gates, the select-gate having a portion between the first and second floating gates, the portion of the select-gate extending over a third portion of the channel region between the first and second channel portions, wherein the first, second, and third portions of the channel region do not overlap and together form the entire channel region;

an inter-polysilicon dielectric layer insulating the first and second floating gates from the select-gate, the inter-polysilicon dielectric layer being thinnest between the sharp edge of each of the two floating gates and the select-gate; and

a gate-dielectric layer insulating the first and second floating gates and the portion of the select-gate from the underlying channel region and the first and second junctions,

wherein the cells are serially connected along each row, the select-gates of the cells along each row being connected together forming a wordline, the first junction of the cells along each column being connected together forming a continuous bitline, and the second junction of the cells along each column being connected together forming another continuous bitline.

29. The cell structure of Claim 28 wherein in a programming cycle, at least one of the plurality of rows is selected while all other rows are unselected, the

unselected rows being biased to ground or a negative voltage.

30. A method of forming a memory cell, the method comprising:

forming a first junction and a second junction in a body region, the first and second junctions being separated by a channel region;

forming a first floating gate and a second floating gate over the channel region, each of the first and second floating gates having at least one slanted surface forming a sharp edge; and

forming a select-gate over at least a portion of each of the first and second floating gates, the select-gate having a portion between the first and second floating gates.

31. The method of Claim 30 wherein the first floating gate extends over a first portion of the channel region and over a portion of the first junction, and the second floating gate extends over a second portion of the channel region and over a portion of the second junction.

32. The method of Claim 31 wherein the portion of the select-gate extends over a third portion of the channel region between the first and second channel portions.

33. The method of Claim 32 wherein the first, second, and third portions of the channel region do not overlap, and the first, second, and third channel portions together form the entire channel region between the first and second junctions.

34. The method of Claim 30 further comprising forming an inter-polysilicon dielectric layer for

insulating the first and second floating gates from the select-gate, the inter-polysilicon dielectric layer being thinnest between the sharp edge of each of the two floating gates and the select-gate.

35. The method of Claim 30 further comprising:

forming an insulating layer for insulating the first and second floating gates from their underlying channel regions; and

forming an insulating layer for insulating the select-gate from its underlying channel region.

36. The method of Claim 30 wherein the body region is either a p-type substrate or an internal p-well, the internal p-well being formed in a n-type well, the n-type well being formed in a p-type substrate.

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